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First Inventor or Application Identifier Kohei ABE

Title QUEUE CONTROL DEVICE FOR AND QUEUE CONTROL METHOD OF CONTROLLING A PLURALITY OF QUEUES

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09/19/00**APPLICATION ELEMENTS**

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2.  Specification Total Pages **25**
3.  Drawing(s) (35 U.S.C. 113) Total Sheets **7**  
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in the prior application, see 37 C.F.R. §1.63(d)(2) and  
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Filed on
- This application claims priority of provisional application Serial No. Filed

**17. CORRESPONDENCE ADDRESS****22850**(703) 413-3000  
FACSIMILE: (703) 413-2220

Name:	Marvin J. Spivak	Registration No.:	24,913
Signature:		Date:	9/19/00
Name:	C. Irvin McClelland Registration Number 21,124	Registration No.:	

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INVENTOR(S) Kohei ABE

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FOR: QUEUE CONTROL DEVICE FOR AND QUEUE CONTROL METHOD OF CONTROLLING A PLURALITY OF QUEUES

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Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,  
MAIER & NEUSTADT, P.C.

C. Irvin McClelland

Marvin J. Spivak  
Registration No. 24,913

**C. Irvin McClelland**  
**Registration Number 21,124**

Date: 9/19/00



**22850**

Tel. (703) 413-3000  
Fax. (703) 413-2220  
(OSMMN 11/98)

TITLE OF THE INVENTION

QUEUE CONTROL DEVICE FOR AND QUEUE CONTROL METHOD OF  
CONTROLLING A PLURALITY OF QUEUES

CROSS-REFERENCE TO RELATED APPLICATIONS

5        This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 11-273219, filed September 27, 1999, the entire contents of which are incorporated herein by reference.

10        BACKGROUND OF THE INVENTION

This invention relates to a queue control device and a queue control method which are applied to, for example, ATM (Asynchronous Transfer Mode) communications and computers.

15        FIG. 7 shows a conventional queue management method. The queue management method includes a pointer table 101 having an n number of addresses and a storage area 102 that stores the head address and tail address for the queue in the pointer table 101. When a queue is constructed for an n number of elements, address A0 to address An are allocated to the individual elements in the pointer table 101. In each address in the pointer table 101, pointer information indicating the next element for constituting the queue is stored. The 20        storage area 102 stores the head address and tail address. The head address indicates the head element in the queue in the pointer table 101 and the tail 25

address indicates the tail element. Using these addresses, the queue is managed.

For example, in the example of FIG. 7, address A0 in the pointer table has been stored in the head address in the storage area 102 and address A7 has been stored in the tail address. In address A0 in the pointer table 101 indicated by the head address, pointer information A2 indicating the address for the next element has been stored. Furthermore, pointer information A8 indicating the address for the next element has been stored in address A2 in the pointer table 101 and pointer information A7 indicating the tail address is stored in address A8 in the pointer table 101. Since address A7 in the pointer table 101 is the tail address, it has no next pointer information and has 0 indicating the end of the queue stored in it. In this way, a queue consisting of addresses A0 → A2 → A8 → A7 is constructed.

The queue is accessed sequentially, starting at address A0. After the process corresponding to address A0 has been completed, the pointer information corresponding to address A0 is deleted from the queue and the head address is updated from A0 to A2.

There are two methods of adding new elements to the queue as follows. When element Ai is added to an FIFO (First In First Out) queue, pointer information indicating Ai is stored in the tail address A7 of the

pointer table 101 and the tail address of the storage area 102 is updated from A7 to Ai. On the other hand, when element Ai is added to an LIFO (Last In First Out) queue, pointer information indicating the head address A0 is stored in Ai of the table 101 and the head address of the storage area 102 is updated from A0 to Ai.

FIG. 8 shows a queue management method for managing two types of queues. To manage a first and a second queue, two storage areas 111, 112 are provided. The storage area 111 holds the head address 1 and tail address 1 in the first queue. The first queue is managed using the head address 1 and tail address 1. The storage area 112 holds the head address 2 and tail address 2 in the second queue. The second queue is managed using the head address 2 and tail address 2.

Now, consider a case where queues are managed in a communication control system with, for example, an n number of communication channels. For example, in ATM communications, virtual channels are shared on one physical line, and packet is changed into ATM cell and transmits in the virtual channel. A bandwidth used by each virtual channel is classified into some groups corresponding to the application of each virtual channel, and each group is controlled according to a priority. That is, channels of each group are managed by the queue and each group is controlled according to

the priority.

FIG. 9 shows the queue management method. In FIG. 9, a time table is provided in a storage area 121. The time table has an  $m$  number of time entries  $T_0$  to  $T_m$ .  
5 Each channel is serviced in this order of  $T_0$  to  $T_m$  of the  $m$  number of entries. In each of the time entries  $T_0$  to  $T_m$ , the head address and tail address of a queue for a virtual channel serviceable at each time have been stored. For example, at time entry  $T_0$ ,  $A_{h1-0}$  (= A0) has been stored in the head address and  $A_{t1-0}$  (= A2) has been stored in the tail address. Moreover, at time entry  $T_1$ ,  $A_{h1-1}$  (= A3) has been stored in the head address and  $A_{t1-1}$  (= A3) has been stored in the tail address.  
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15 On the other hand, according to the head address and tail address at each of the entries, the pointer indicating the next element and information indicating the end have been stored in the pointer table 122.

Each channel is served in order from time entry  $T_0$  20 in the time table. After service has been given at time entry  $T_m$ , service is given, starting at time entry  $T_0$  again. After the virtual channel registered in a certain entry has been given service, the virtual channel is registered in another time entry. If 25 another virtual channel has been registered in that time entry, the virtual entry will constitute a queue at that time entry.

Consider a case where two types of virtual channels differing in priority are controlled in such a communication control device. As shown in FIG. 9, when there is only one queue at time entries T<sub>0</sub> to T<sub>m</sub>, control can be performed only by FIFO or LIFO. This causes a problem: the two types of virtual channels cannot be controlled independently on the basis of their priority.

To overcome this problem, as shown in FIG. 10, a queue control method having two sets of head addresses and tail addresses for each of the time entries T<sub>0</sub> to T<sub>m</sub> is needed. The method is based on the method shown in FIG. 8. In the example shown in FIG. 10, there are a first queue and a second queue for each of the time entries T<sub>0</sub> to T<sub>m</sub>. With the first queue and second queue, two types of virtual channels differing in priority can be controlled as shown in the pointer table 122. Specifically, for example, at time entry T<sub>0</sub>, the first queue specified by the head address Ah1-0 (= A<sub>0</sub>) and tail address At1-0 (= A<sub>2</sub>) is processed. Then, the second queue specified by the head address Ah2-0 (= A<sub>1</sub>) and tail address At2-0 (= A<sub>5</sub>) is processed.

As shown in FIG. 10, however, when two types of queues composed of the first queue and second queue are managed using the m number of time entries T<sub>0</sub> to T<sub>m</sub>, the storage area 123 requires an area for storing 4 × m head addresses and tail addresses. This leads to a

problem: the storage capacity of the storage area 123 increases.

BRIEF SUMMARY OF THE INVENTION

It is, accordingly, an object of the present  
5 invention to overcome the above problem by providing a queue control device and a queue control method which are capable of preventing the storage capacity from increasing by controlling a plurality of queues as a single queue.

10 The foregoing object is accomplished by providing a queue control device comprising: a first storage area for storing a first and a second queue, the first queue including a plurality of elements, each of the elements having an address specifying the next element, and the second queue including a plurality of elements, each of the elements having an address specifying the next element; a second storage area for storing first pointer information and second pointer information, the first pointer information being a head address  
15 specifying the head element in the first queue, and the second pointer information being a tail address specifying the tail element in the second queue; and a controller which controls the first and second storage areas and which sets not only an address specifying the head element in the second queue in the tail element in the first queue stored in the first storage area but also an address specifying the tail address in the  
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first queue in the tail element in the second queue and controls the first and second queues according to the first pointer information and second pointer information stored in the second storage area.

5       The foregoing object is further accomplished by providing a queue control method including a first queue composed of a plurality of elements, each of the elements having an address specifying the next element, and a second queue composed of a plurality of elements, 10 each of the elements having an address specifying the next element, the queue control method comprising the steps of: setting an address specifying the head element in the second queue in the tail element in the first queue; setting an address specifying the tail 15 element in the first queue in the tail element in the second queue; processing the first and second queues on the basis of first pointer information made up of the head address in the first queue and second pointer information made up of the tail address in the second 20 queue.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and 25 advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out hereinafter.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention, and together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

FIG. 1 is a diagram showing a queue control method according to an embodiment of the present invention;

FIG. 2 is a diagram showing a queue control method when there is no second queue in the present invention;

FIG. 3 is a diagram showing a queue control method when there is no first queue in the present invention;

FIG. 4 is a diagram showing a method of controlling two sets of queues using a plurality of time entries in the present invention;

FIG. 5 shows the configuration of an embodiment of a queue control device according to the present invention;

FIGS. 6A and 6B are flowcharts for the operation of the control circuit of FIG. 5;

FIG. 7 is a diagram showing a conventional basic queue control method;

FIG. 8 is a diagram showing a conventional basic method of controlling two queues;

FIG. 9 is a diagram showing a conventional method

of controlling a single queue using a plurality of time entries; and

FIG. 10 is a diagram showing a conventional method of controlling two queues using a plurality of time entries.

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#### DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, referring to the accompanying drawings, an embodiment of the present invention will be explained.

10 FIG. 1 shows the structure of a queue according to the present invention. In FIG. 1, the elements constituting a first and a second queue have been stored in a pointer table 11. Specifically, the elements of the first queue have been stored in addresses A0, A2, A7, and A8 and the elements of the second queue have been stored in addresses A3, A4, and A6. In each address, pointer information indicating the address for the next address has been stored. That is, the first queue is composed of A0 → A2 → A8 → A7 and the second queue is composed of A6 → A4 → A3. In this case, the head address A6 in the second queue is stored as pointer information in the tail address A7 in the first queue and the tail address A7 in the first queue is stored as pointer information in the tail address A3 in the second queue.

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In a storage area 12, the head address and tail address are stored. Pointer information indicating the

head address A0 in the first queue is stored in the head address and pointer information indicating the tail address A3 in the second queue is stored in the tail address.

5       With such a structure, the first and second queues can be constructed into a single queue. Moreover, the first and second queues can be processed using only a set of the head address and tail address stored in the storage area 12. Specifically, after the first queue  
10      has been processed according to the head address stored in the storage area 12, the second queue can be processed automatically.

When the first queue and second queue need to be separated, pointer information A7 stored in address A3 in the pointer table 11 indicated by the tail address A3 in the storage area 12 is read. Then, pointer information A6 stored in the address A7 specified by pointer information A7 is taken out. This makes it possible to distinguish the end of the first queue and the beginning of the second queue. As a result, the first queue consisting of the head address A0 → A2 → A8 → A7 can be separated from the second queue consisting of pointer information A6 to the tail address A3, or A6 → A4 → A3. After the first and second queues have been separated, each of the first and second queues can be subjected to an FIFO or LIFO process. When the first and second queues need to be  
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connected again into a single queue, they have only to be connected again by the method of the present invention.

For example, when only the first queue is present  
5 as shown in FIG. 2, A0 representing the head address in the first queue is stored as pointer information in the head address in the storage area 12 and A7 representing the tail address in the first queue is stored as pointer information in the tail address. Pointer  
10 information indicating that only the first queue is present, for example, "0," is set in A7 representing the tail address in the pointer table 11.

On the other hand, when only the second queue is present as shown in FIG. 3, A6 representing the head address in the second queue is stored as pointer information in the head address in the storage area 12 and A3 representing the tail address in the second queue is stored as pointer information in the tail address. The value indicating that only the second  
15 queue is present, for example, pointer information "A3"  
20 about the tail address A3, is set in A3 representing the tail address in the pointer table 11.

With this structure, two queues can be managed using a set of the head address and tail address.

25 FIG. 4 shows a case where virtual-channel queues differing in priority are managed using the present invention in a communication control system with, for

example, an n number of communication channels.

In FIG. 4, numeral 21 indicates a pointer table and 22 indicates a storage area. In the storage area 22, a time table 22a is provided. The time table 22a have an m number of time entries T0 to Tm. Each channel is serviced in this order of T0 to Tm of the m number of entries. In each of the time entries T0 to Tm, the head address and tail address of a queue for a virtual channel serviceable at each time have been stored.

For example, at time entry T0, pointer information Ah1-0 (= A0) representing the head address in the first queue ( $A_0 \rightarrow A_2$ ) with a first priority has been stored in the head address. In the tail address, pointer information At1-0 (= A5) representing the tail address in the second queue ( $A_1 \rightarrow A_5$ ) with a second priority lower in level than the first priority has been stored. In address A5 in the pointer table 21, pointer information A2 representing the tail address in the first queue with the first priority has been stored.

Moreover, at time entry T1, pointer information Ah1-1 (= A3) representing the head address in the first queue ( $A_3 \rightarrow A_8$ ) has been stored in the head address. In the tail address, pointer information At1-1 (= A8) representing the tail address in the second queue ( $A_7 \rightarrow A_3$ ) has been stored. In address A3 in the pointer table 21, pointer information A8 representing

the tail address in the first queue has been stored.

By constructing the time table 22a in the storage area 22 and the pointer table 21 as described above,  $2 \times M$  sets of head addresses and tail addresses are required for an  $m$  number of time entries in the present embodiment, when the first and second virtual-channel queues differing in priority are managed, as compared with a conventional equivalent where  $4 \times M$  sets of head addresses and tail addresses are required for an  $m$  number of time entries. Because in the embodiment, the two queues can be controlled only by the head addresses and tail addresses used to control a single queue, the capacity of the storage area 22 can be reduced to 1/2 of that shown in FIG. 10.

Conversely, in a case where a queue for a low-priority communication channel is made up of the first queue and a queue for a high-priority communication channel is made up of the second queue and then these queues are connected as described above into a single queue, the first and second queues are separated by the above method according to the head addresses and tail addresses registered in the  $m$  number of time entries, which enables service to be given by the communication channel registered in the first queue with the high priority.

FIG. 5 shows an embodiment of a queue control device applied to the present invention. In FIG. 5, a

first memory 31 is composed of, for example, a RAM (random access memory). The first memory 31 corresponds to, for example, the storage area 22 shown in FIG. 4 and stores the time table 22a. A second memory 32 is composed of, for example, a RAM, and stores, for example, the pointer table 21 shown in FIG. 4. A control circuit 33 is composed of, for example, a microprocessor. The control circuit 33 subjects the time table 22a and the first and second queues in the pointer table 21 to the processes shown in FIGS. 1 to 3.

FIGS. 6A and 6B show the operation of the control circuit 33.

When the first and second queues are present, pointer information specifying the head element in the second queue is set in the tail element in the first queue in the pointer table 21. In the tail element in the second queue, pointer information specifying the tail element in the first queue is set. Moreover, the address specifying the head element in the first queue is stored as a head address in the time table 22a and the address specifying the tail element in the second queue is stored as a tail address in the time table 22a (ST1 to ST6).

When the first queue is absent, the address specifying the head element in the second queue is stored as a head address in the time table 22a. In

addition, pointer information indicating that the first queue is absent is set in the tail element in the second queue in the pointer table 21 (ST1, ST7 to ST9).

When the second queue is absent, the address  
5 specifying the tail element in the first queue is stored as a tail address in the time table 22a. In addition, pointer information indicating that the second queue is absent is set in the tail element in the first queue in the pointer table (ST2, ST10, ST11).

10 The control circuit 33 accesses sequentially the time table 22a stored in the first memory 31. Then, according to the head address and tail address stored in each of the time entries, the control circuit accesses the queue in the pointer table 21 stored in  
15 the second memory 32 and outputs, for example, the number of a virtual channel.

Specifically, the control circuit reads the head address ( $Ah_n$ ) and tail address ( $At1_n$ ) at, for example, time  $Tn$  from the first memory 31 and judges whether or  
20 not a queue is present (ST21, ST22). If the result of the judgment has shown that there is no queue, a virtual channel will not be transmitted (ST23).

On the other hand, if the result of the judgment has shown that there is a queue, the controller reads  
25 the pointer information ( $Ap$ ) in the tail address ( $At1_n$ ) from the second memory 32 (ST24). The control circuit judges whether the pointer information ( $Ap$ )

indicates only the first queue (ST25). If the result of the judgment has shown that only the first queue is indicated, the control circuit accesses the first queue (Ah1\_n) sequentially and selects the corresponding virtual channel from the second memory 32 (ST26).

5 If in step ST25, the result has shown that the pointer information (Ap) does not indicate only the first queue, the control circuit judges whether the pointer information (Ap) indicates only the second queue (ST27). If the result of the judgment has shown that only the second queue is indicated, the control circuit accesses the second queue (Ah1\_n) sequentially and selects the corresponding virtual channel from the second memory 32 (ST28).

10 15 If in step ST27, the result has shown that the pointer information (Ap) does not indicate only the second queue, the control circuit reads the pointer information (Ap) in the pointer (Ap) from the second memory 32 (ST29). Thereafter, the control circuit separates the queue into the first queue (Ah1\_n to Ap) and second queue (Ap to At1\_n) (ST30). Then, the control circuit accesses the higher-priority queue, in this case, the first queue, sequentially and selects the corresponding virtual channel from the second memory 32 (ST26).

20 25 The number of the virtual channel outputted from the control circuit 13 is supplied to the transmission

control circuit 34. The transmission control circuit 34 outputs the virtual channel corresponding to the number of the virtual channel.

5       The first memory 31, control circuit 33, and transmission control circuit 34 have been provided in, for example, a single semiconductor chip 35. The second memory 32 has been provided on a separate semiconductor chip. The second memory 32 may be provided integrally in the semiconductor chip 35.

10      With the embodiment, a set of pointer information about the head address and pointer information about the tail address enables two queues to be controlled according to their priority. This prevents the storage area for storing head addresses and tail addresses from increasing, as compared with a case where the queues are controlled using pointer information about a plurality of head addresses and pointer information about a plurality of tail addresses.

15      Furthermore, even when one of the first and second queues in a set, or one of the first and second queues separated is gone during the processing, the head address and tail address in the storage area can control the remaining queue.

20      Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments

shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

the first time in the history of the world, the people of the United States have been compelled to go to war to defend their country.

WHAT IS CLAIMED IS:

1. A queue control device comprising:

a first storage area for storing a first and a second queue, said first queue including a plurality of elements, each of said elements having an address specifying the next element, and said second queue including a plurality of elements, each of said elements having an address specifying the next element;

5                   a second storage area for storing first pointer information and second pointer information, said first pointer information being a head address specifying the head element in said first queue, and said second pointer information being a tail address specifying the tail element in said second queue; and

10                  a controller which controls said first and second storage areas and which sets not only an address specifying the head element in said second queue in the tail element in said first queue stored in said first storage area but also an address specifying the tail address in said first queue in the tail element in said second queue and controls said first and second queues according to said first pointer information and second pointer information stored in said second storage area.

20                  2. The queue control device according to claim 1, 25 wherein said controller, when said first queue is absent, sets not only an address specifying the head element in said second queue as said first pointer

information in said second storage area but also first information indicating that said first queue is absent in the tail element in said second queue in said first storage area.

5       3. The queue control device according to claim 1, wherein said controller, when said second queue is absent, sets not only an address specifying the tail element in said first queue as said second pointer information in said second storage area but also second information indicating that said second queue is absent in the tail element in said first queue in said first storage area.

10      4. The queue control device according to claim 1, wherein said second storage area stores a plurality of pieces of said first pointer information and a plurality of pieces of said second pointer information.

15      5. The queue control device according to claim 1, wherein said first queue is given higher priority than said second queue.

20      6. The queue control device according to claim 1, wherein said first storage area stores the number of a virtual channel according to each of said elements.

25      7. The queue control device according to claim 1, wherein said controller is connected to a transmission controller, said transmission controller outputting a virtual channel according to said number of a virtual channel supplied from said controller.

8. A queue control device comprising:

a first storage area for storing a plurality of queue groups, each of said queue groups including a first and a second queue, each of said first and second queues having a plurality of elements, each of said elements in said first and second queues holding an address specifying the next element;

a second storage area for storing a time table, said time table including a plurality of time entries, each of said time entries having first pointer information and second pointer information, said first pointer information being a head address specifying the head element in said first queue in each of said queue groups and said second pointer information being a tail address specifying the tail element in said second queue in each of said queue groups; and

a controller which controls said first and second storage areas and which sets not only an address specifying the head element in said second queue in the tail element in said first queue in each of said queue groups stored in said first storage area but also an address specifying the tail element in said first queue in the tail element in said second queue and controls each of said first and second queues according to said first pointer information and second pointer information.

9. The queue control device according to claim 8,

wherein said controller, when said first queue is absent in each of said queue groups, sets not only an address specifying the head element in said second queue as said first pointer information in said second storage area but also first information indicating that said first queue is absent in the tail element in said second queue in said first storage area.

10. The queue control device according to claim 8, wherein said controller, when said second queue is absent in each of said queue groups, sets not only an address specifying the tail element in said first queue as said second pointer information in said second storage area but also second information indicating that said second queue is absent in the tail element in said first queue in said first storage area.

11. The queue control device according to claim 8, wherein said first queue is given higher priority than said second queue in each of said queue groups.

12. The queue control device according to claim 8, wherein said first storage area stores the number of a virtual channel according to each of said elements in each of said queue groups.

13. The queue control device according to claim 8, wherein said controller is connected to a transmission controller, said transmission controller outputting a virtual channel according to said number of a virtual channel supplied from said controller.

14. A queue control method including a first queue composed of a plurality of elements, each of said elements having an address specifying the next element, and a second queue composed of a plurality of elements, 5 each of said elements having an address specifying the next element, the queue control method comprising the steps of:

10 setting a head address specifying the head element in said second queue in the tail element in said first queue;

setting a tail address specifying the tail element in said first queue in the tail element in said second queue;

15 processing said first and second queues on the basis of first pointer information made up of the head address in said first queue and second pointer information made up of the tail address in said second queue.

16. The queue control method according to claim 14, 20 further comprising the step of, when said first queue is absent, setting not only an address specifying the head address in said second queue as said first pointer information but also first information indicating that said first queue is absent in the tail element in said second queue.

25 16. The queue control method according to claim 14, further comprising the step of, when said second queue

is absent, setting not only an address specifying the tail address in said first queue as said second pointer information but also second information indicating that said second queue is absent in the tail element in said first queue.

5           17. The queue control method according to claim 14, wherein the priority of said first queue is set higher than that of said second queue.

10          18. The queue control method according to claim 14, wherein said elements in said first and second queues are allocated the numbers of virtual channels in a one-to-one correspondence.

DOCUMENT NUMBER

## **ABSTRACT OF THE DISCLOSURE**

In the tail address in a first queue in a pointer table, the head address in a second queue is stored as pointer information. In the tail address in the second queue, the tail address in the first queue is stored as pointer information. Pointer information about the head address in the first queue is stored in the head address in a storage area. In the tail address, pointer information about the tail address in the second queue is stored.

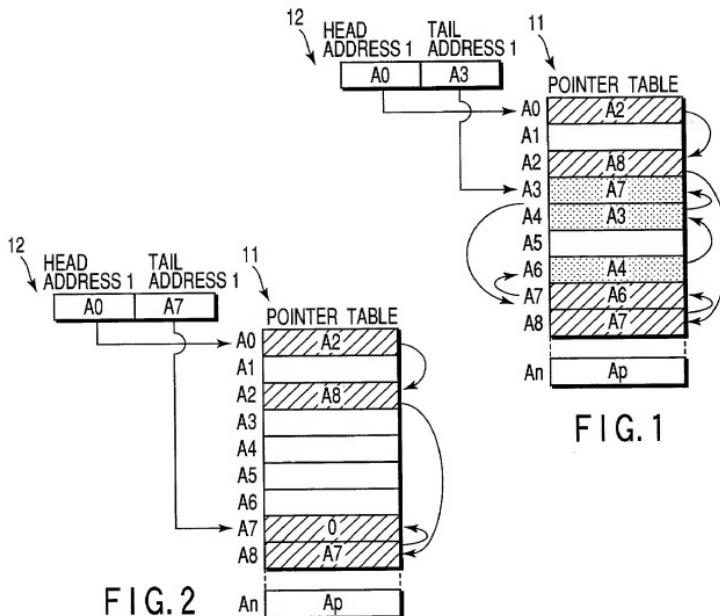


FIG. 1

FIG. 2

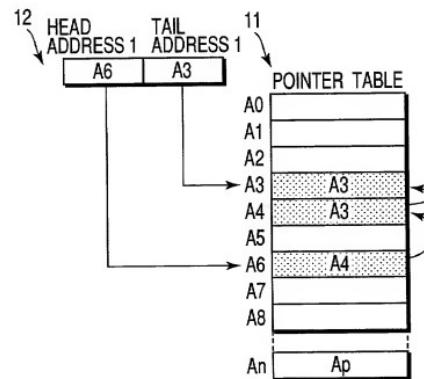


FIG. 3

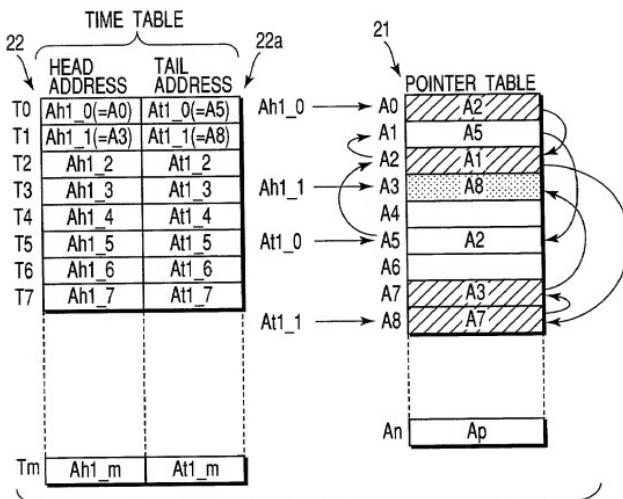


FIG. 4

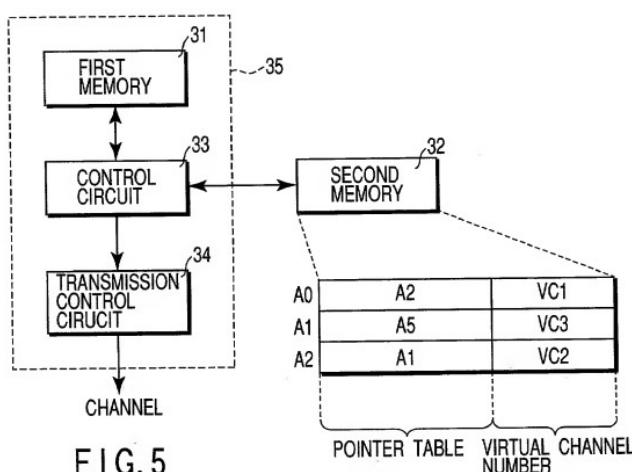


FIG. 5

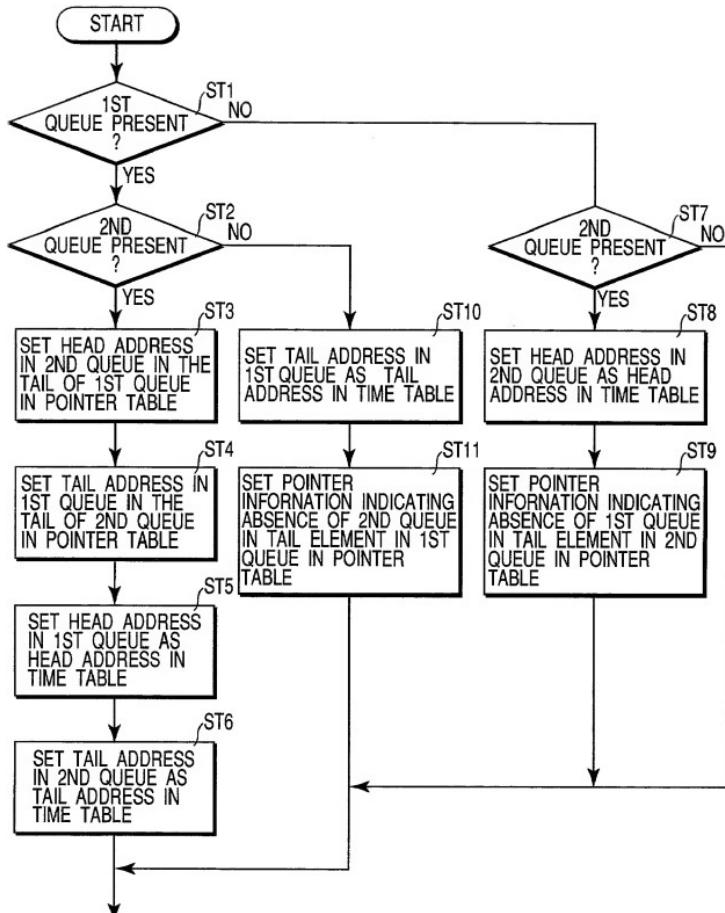


FIG. 6A

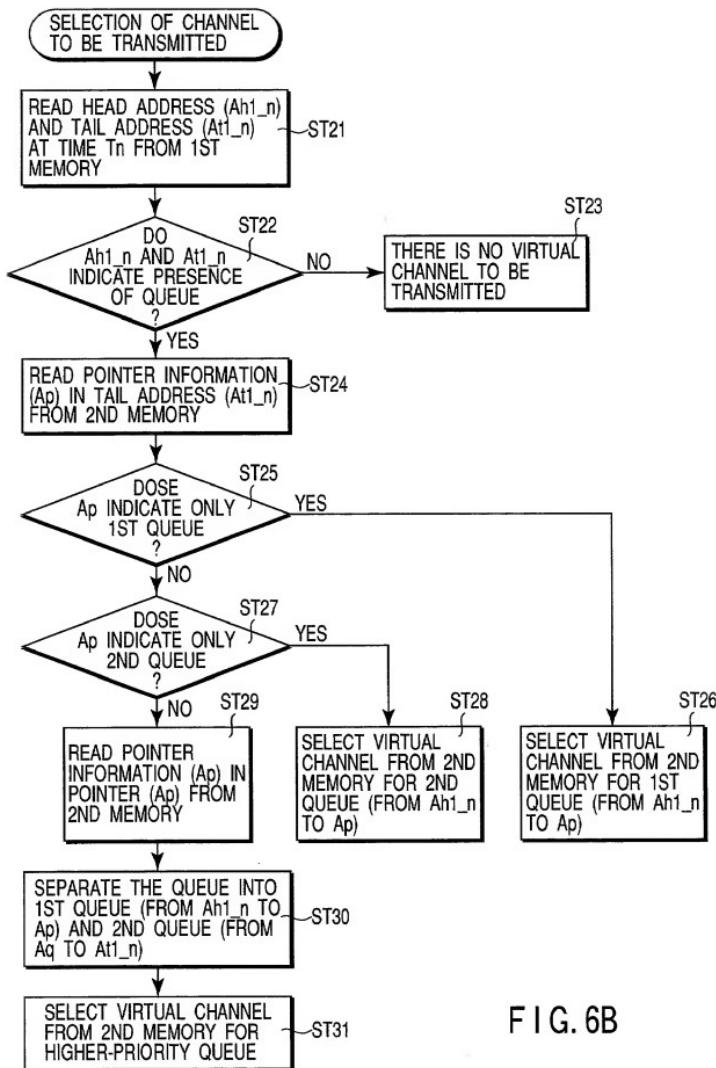


FIG. 6B

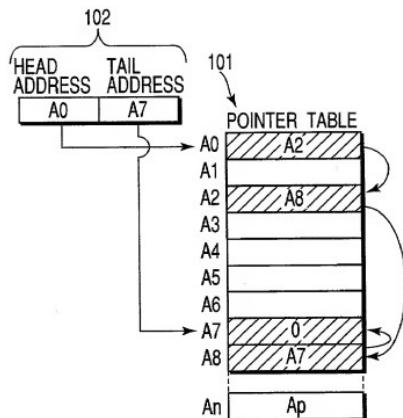


FIG. 7

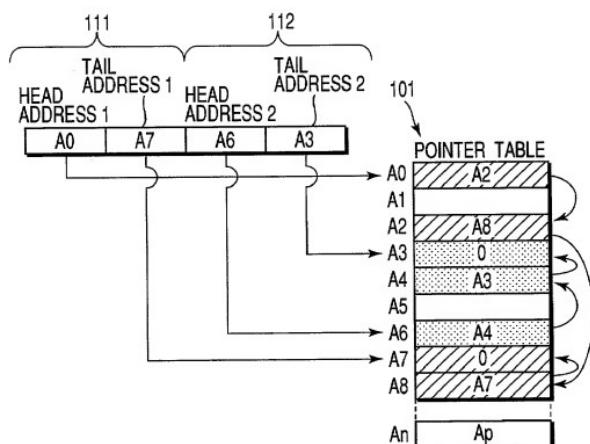
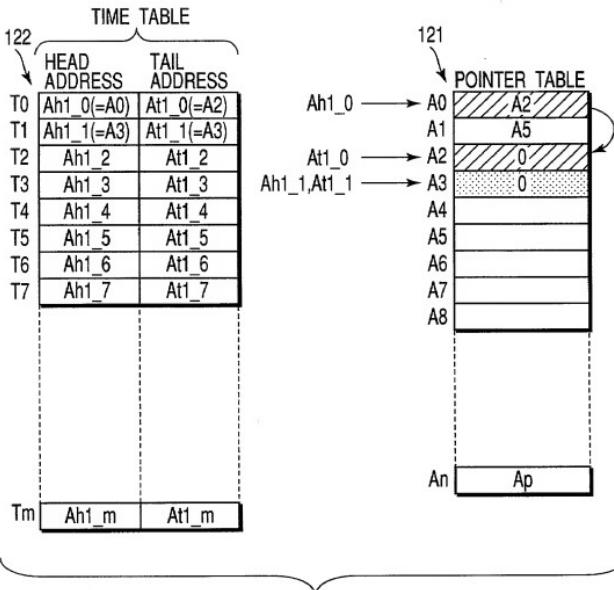
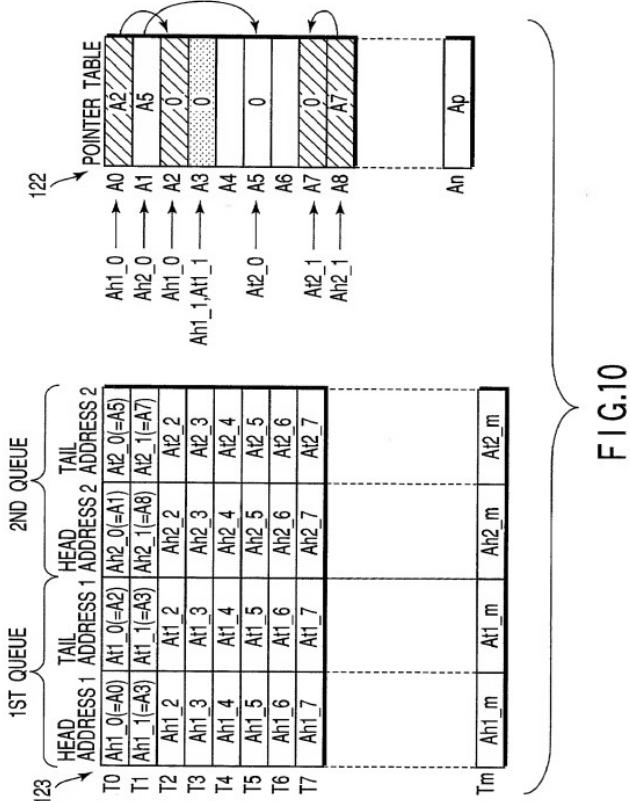


FIG. 8





## DECLARATION FOR PATENT APPLICATION

As a below named inventor, I declare: that I verify believe myself to be the original, first and sole (if only one individual inventor is listed below) or an original, first and Joint Inventor (if more than one individual inventor is listed below) of the invention in

QUEUE CONTROL DEVICE FOR AND QUEUE CONTROL METHOD OF  
CONTROLLING A PLURALITY OF QUEUES

the specification of which is attached hereto unless the following box is checked.

was filed on \_\_\_\_\_ as United States Application  
or PCT International Application No. \_\_\_\_\_, and  
was amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information of which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365 (b) of any foreign application(s) for patent or inventor's certificate, or 35 U.S.C. 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

<u>Country</u>	<u>Category</u>	<u>Application No.</u>	<u>Filing Date</u>	<u>Priority Claim</u>
Japan	Patent	11-273219	September 27, 1999	Yes

And I hereby appoint Norman F. Oblon (Reg. No. 24,618), Marvin J. Spivak (Reg. No. 24,913), C. Irvin McClelland (Reg. No. 21,124), Gregory J. Maier (Reg. No. 25,599), Arthur I. Neustadt (Reg. No. 24,854), Richard D. Kelly (Reg. No. 27,757), James D. Hamilton (Reg. No. 28,421), Eckhard H. Kuesters (Reg. No. 28,870), Robert T. Pous (Reg. No. 29,099), Charles L. Gholz (Reg. No. 26,395), Vincent J. Sunderdick (Reg. No. 29,004), William E. Beaumont (Reg. No. 30,996), Robert F. Gnuse (Reg. No. 27,295), Jean-paul Lavallee (Reg. No. 31,451), Stephen G. Baxter (Reg. No. 32,884), Robert W. Hahl (Reg. No. 33,893), Richard L. Treanor (Reg. No. 36,379), Steven P. Weihrouch (Reg. No. 32,829), John T. Goolkasian (Reg. No. 26,142), Richard L. Chino (Reg. No. 34,305), Steven E. Lipman (Reg. No. 31,011), Carl E. Schlier (Reg. No. 34,426), James J. Kulbaski (Reg. No. 34,648), Richard A. Neifeld (Reg. No. 35,299), J. Derek Msaon (Reg. No. 35,270), Surinder Sachar (Reg. No. 34,423), Christina M. Gadiano (Reg. No. 37,628), Jeffrey B. McIntyre (Reg. No. 36,867), Paul E. Rauch (Reg. No. 38,591), William T. Enos (Reg. No. 33,128) and Michael E. McCabe, Jr. (Reg. No. 37,182) each of whose address is Fourth Floor, 1755 Jefferson Davis Highway, Arlington, Virginia 22202, or any one of them, my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent & Trademark Office connected therewith, and request that correspondence be directed to Oblon, Spivak, McClelland, Maier & Neustadt, P.C., Fourth Floor, 1755 Jefferson Davis Highway, Arlington, Virginia 22202.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

## DECLARATION FOR PATENT APPLICATION

I declare further that my post office address is at c/o Intellectual Property Division, KABUSHIKI KAISHA TOSHIBA, 1-1 Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan; and that my citizenship and residence are as stated below next to my name:

Inventor: (Signature)

Date

Residence

Date: SEP.-8.2000

*Kohei Abe*

Kohel Abe

Citizen of: Japan Yokohama-shi, Japan

Date:

Citizen of: Japan